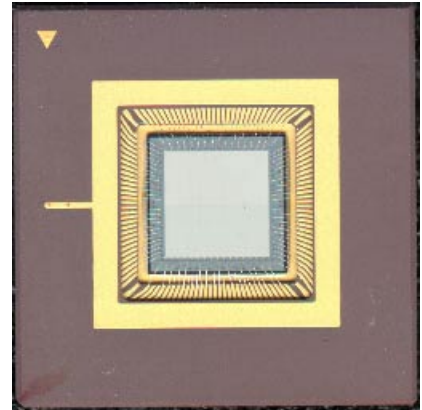




FEATURES

- **512 x 512 Photosite Array**
- **17 μ m x 17 μ m Pixel Size**
- **8.70 mm x 8.70 mm Active Image Area**
- **512 x 512 Optically Active Pixels**
- **19 % Fill Factor**
- **Over 1000 FPS Capable**
- **Anti-blooming to 1000X**
- **Electronic Shuttering VOD Design**
- **Two Phase Buried Channel NMOS**
- **Optional Color Operation Configurable**



GENERAL DESCRIPTION

The CCD456 is a 512 x 512 element solid state Charge Coupled Device (CCD) Interline image sensor which is intended for use in high frame rate scientific, industrial, and commercial electro-optical systems. The CCD456 is organized as a matrix of 32 separate segments of 32 horizontal by 256 vertical CCD photosites. The pixel pitch and spacing is 17 μ m.

The imaging array is operated with vertically strapped phases (one tri-level) which clock charge towards upper and lower serial readout registers. Serial register clocks operate from 0 to 5 volt clock levels to simplify high speed readout schemes. Both vertical and horizontal channels operate in Buried Channel mode. A Summing Gate is provided in each of the 8 output sections for pixel binning if required. The Buried Channel operation offers excellent charge transfer efficiencies even at high readout speeds. An additional implant under each vertical and horizontal phase creates a barrier which allows electrons to be stored under the other non-barrier phases. Dark current is approximately 1 nA/cm² @ 20°C. Excellent antiblooming performance is achieved by use of a vertical overflow drain (VOD) CCD structure. A three stage low noise output amplifier with an output conversion gain of 2.5 μ V/e is utilized in each of the 32 separate outputs. Device processing is done using

1.0 micron design rules. The double metal, two-poly process allows a photosite layout with small pixel geometry and minimal array blemishes.

FUNCTIONAL DESCRIPTION

The CCD456 consists of the following functional elements illustrated in the block diagram.

Image Sensing Elements: Incident photons pass through a transparent oxide layer over each photodiode pixel gate structure creating electron hole pairs. The resulting photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of individual photodiode elements coupled to adjacent vertical interline storage areas. These shielded storage areas are also used to shift image data vertically. Consequently, the device does not need to be shuttered during readout of each sequential frame.

Vertical Charge Shifting: The Interline architecture of the CCD456 provides video information as a parallel sequential readout of 256 lines, each containing 32 photosite elements. At the end of an integration period the ΦV_1 phase is tri-level clocked followed by conventional ΦV_1 and ΦV_2 clocks to transfer charge vertically through the CCD interline array to the horizontal readout register. Vertical columns are separated by channel stop regions to prevent charge migration.

The imaging area is divided into 32 segments (16-upper and 16-lower). Each segment is simultaneously clocked to provide 32 output parallel pixel information.

The last clocked gate in the Horizontal registers (ΦSW) is larger than the others and can be used to horizontally bin charge. This gate can be clocked independently or tied to ΦH_1 for binned or normal full resolution pixel information. The output video is available following the high to low transition of ΦSW .

Output Amplifier: The CCD456 has 32 separate output amplifiers. They are three-stage FET amplifiers with a reset MOSFET tied to the input gate. Charge packets are clocked to a precharged (sense node) capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the Output V_{OUT} pin. The capacitor is reset with ΦR to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET. The first two output amplifier drains are tied to VDD and the output MOSFET drain (OD) can be tied to VDD or a slightly less positive DC potential. The output sources (OSn) are connected to external load resistors to ground. The OS sources constitute the 32 individual video outputs from the device.

DEFINITION OF TERMS

Charge-Coupled Device-A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks $\phi V_1, \phi V_2$ -The clock signals applied to the vertical transport register. Tri-level V_1 and two level V_2 Vertical clocks are common to all image area groups. This minimizes requirements for external clocking electronics. Color applications utilize the same readout structure with individual R-G-B dye matrix structures over the photosites.

Horizontal Transport Clocks $\phi H_1, \phi H_2$ -The clock signals applied to the horizontal transport registers.

Reset Clock ϕR -The clock applied to the reset switch of the output amplifiers.

Dynamic Range -The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure -The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity -The output signal voltage per unit of exposure.

Spectral Response Range -The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

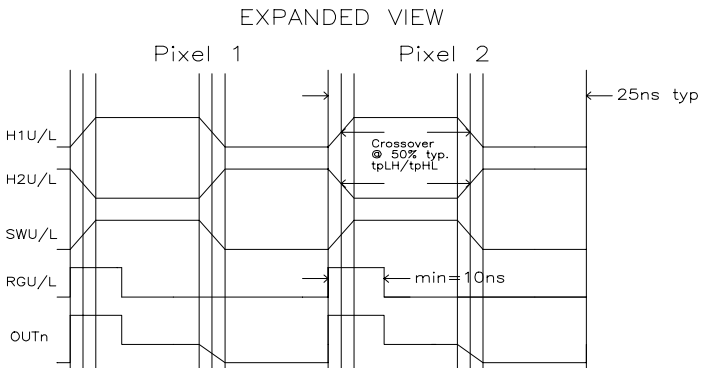
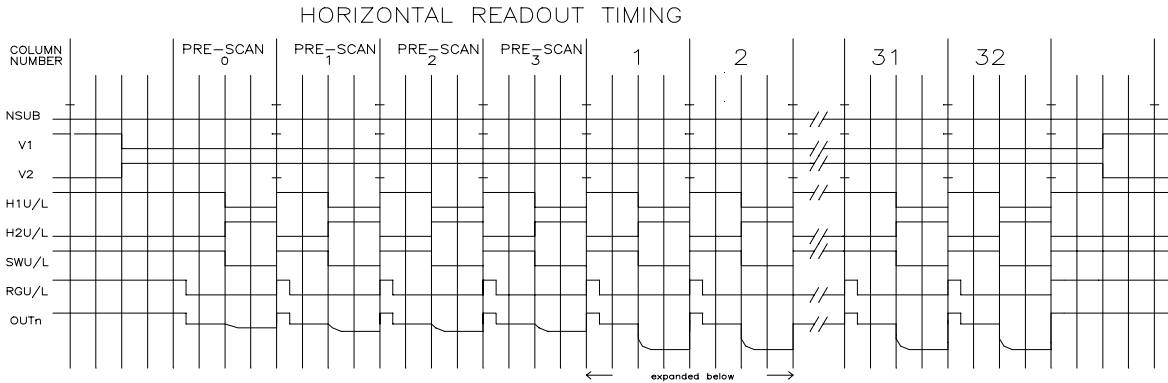
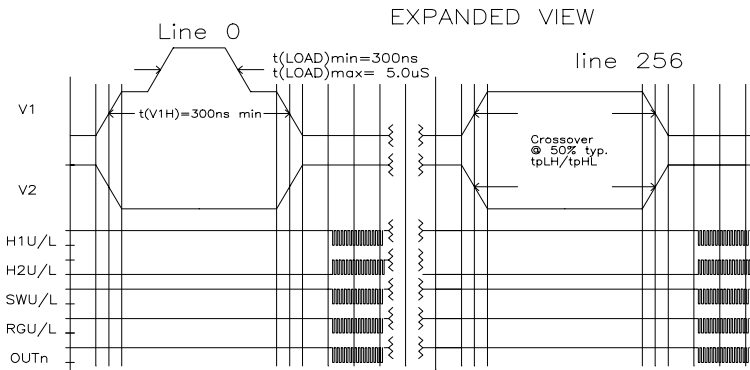
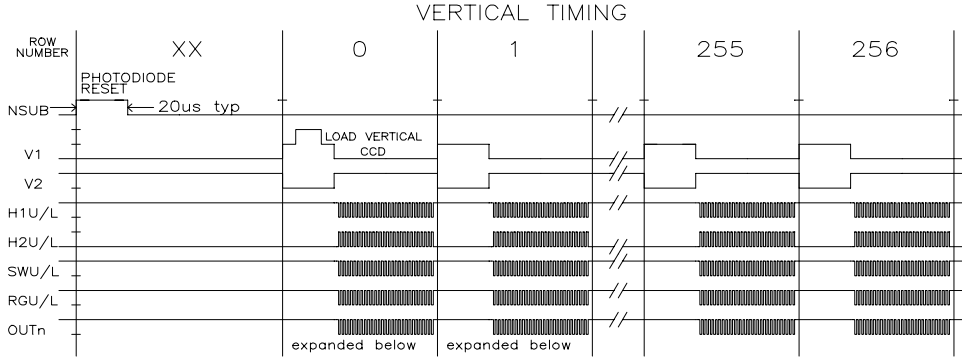
Photo-Response Non-Uniformity -The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal -The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Pixel - Picture element or sensor element also called photoelement, photodiode, or photosite.

CCD456 Timing Diagram

CCD4156 INTERLINE TRANSFER READOUT TIMING
TIMING FOR ALL OUTPUTS—PIXELS ARE PRESENT AT EACH OF 32 OUTPUTS



CCD456 PACKAGE PIN ASSIGNMENTS

(See Package Pin Diagram)

<i>Pin #</i>	<i>Name</i>	<i>Pin #</i>	<i>Name</i>
1	OD	31	OD
2	VDD1	32	N.C.
3	VSRC	33	N.C.
4	VLOAD	34	OS1
5	OTG	35	OS2
6	RD	36	PWELL
7	PWELL	37	OS3
8	RG	38	OS4
9	H2	39	PWELL
10	PWELL	40	OS5
11	H1	41	PWELL
12	SW	42	OS6
13	V1	43	OS7
14	LS	44	PWELL
15	N.C.	45	OS8
16	N.C.	46	OS9
17	LS	47	PWELL
18	V2	48	N.C.
19	SW	49	OS10
20	H1	50	OS11
21	PWELL	51	PWELL
22	H2	52	OS12
23	RG	53	PWELL
24	PWELL	54	OS13
25	RD	55	OS14
26	OTG	56	PWELL
27	VLOAD	57	N.C.
28	VSRC	58	OS15
29	VDD1	59	OS16
30	NSUB	60	NSUB

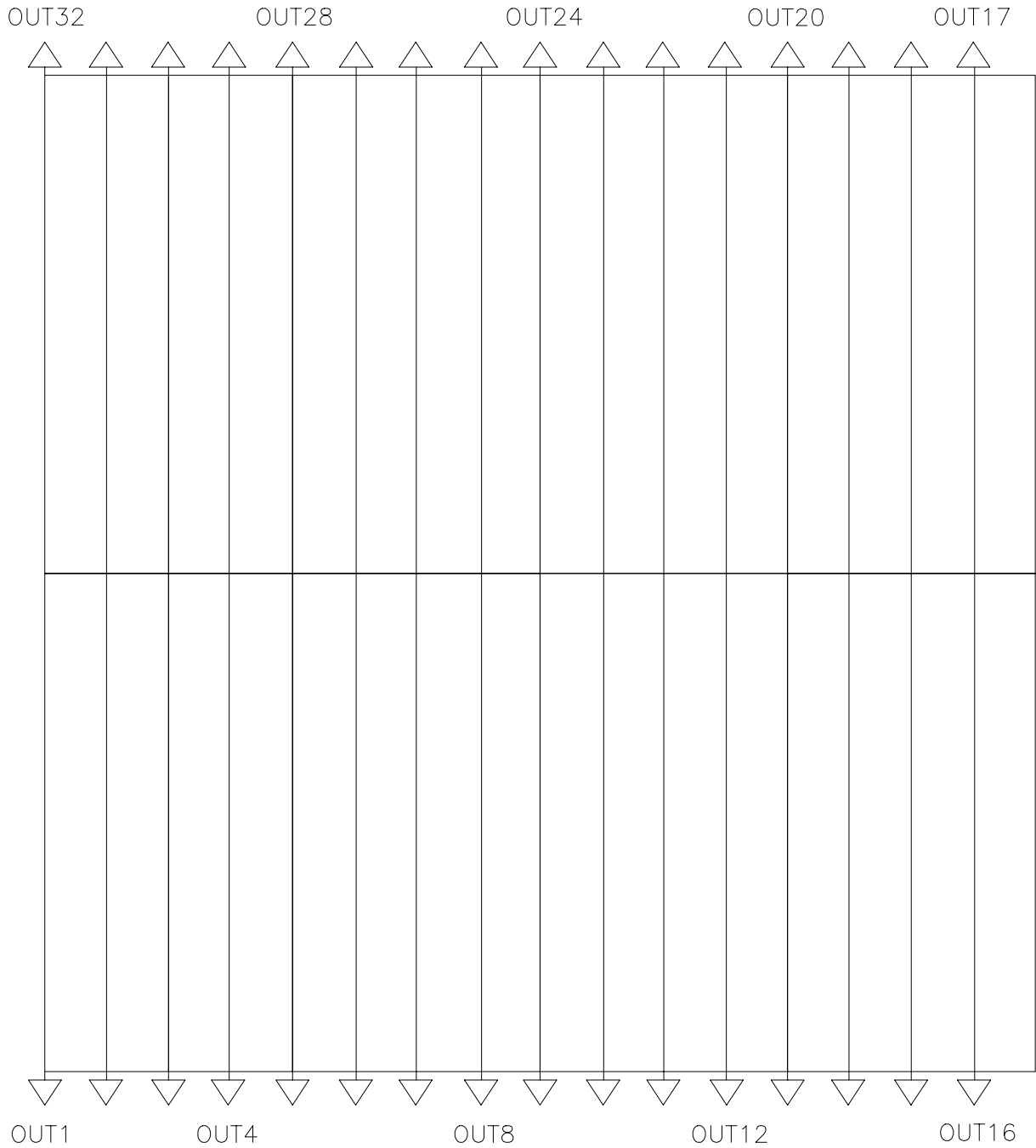
CCD456 PACKAGE PIN ASSIGNMENTS

(See Package Pin Diagram)

<i>Pin #</i>	<i>Name</i>	<i>Pin #</i>	<i>Name</i>
61	OD	91	OD
62	VDD1	92	N.C.
63	VSRC	93	PWELL
64	VLOAD	94	OS32
65	OTG	95	OS31
66	RD	96	PWELL
67	PWELL	97	OS30
68	RG	98	OS29
69	H2	99	PWELL
70	PWELL	100	OS28
71	H1	101	PWELL
72	SW	102	OS27
73	V2	103	OS26
74	LS	104	PWELL
75	N.C.	105	OS25
76	N.C.	106	OS24
77	LS	107	PWELL
78	V1	108	N.C.
79	SW	109	OS23
80	H1	110	OS22
81	PWELL	111	PWELL
82	H2	112	OS21
83	RG	113	PWELL
84	PWELL	114	OS20
85	RD	115	OS19
86	OTG	116	PWELL
87	VLOAD	117	N.C.
88	VSRC	118	OS18
89	VDD1	119	OS17
90	NSUB	120	NSUB

CCD456 IMAGE SEGMENT ARRANGMENT

OUTPUT CONFIGURATION (CCD FACE VIEW)



4156CFGa.DWG

PERFORMANCE CHARACTERISTICS: $T_p = 20^\circ\text{C}$ (Notes 1 & 2)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
DS_{AVE}	Dark Signal, (Readout)		TBD		mV	Note 3
ID_{DARK}	Dark Current Density (Integration)		1.0	2.0	nA/cm ²	Note 3
DS_{NU}	Dark Signal Non-Uniformity		TBD	TBD	mV	Note 4
Q_{Sat}	Full Well Capacity	80	110		Ke ⁻	
V_{Sat}	Saturation Voltage	180	250	400	mV	
PR_{NU}	Photoresponse Nonuniformity			10	% of V_{sat}	Note 5
CTE (V)	Charge Transfer Efficiency, Vertical	.9999	.99995		Per Phase Transfer	
CTE (H)	Charge Transfer Efficiency, Horizontal	.9999	.99995		Per Phase Transfer	
R	Responsivity		TBD		V/ $\mu\text{J}/\text{cm}^2$	
S_{SF}	Sensitivity (Scale Factor)	2.0	2.5		$\mu\text{V}/e^-$	

DC CHARACTERISTICS: $T_p = 20^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{DD1}	DC Supply Voltage	14.7	15	16	Volts	
V_{DD2}	Output Drain Supply Voltage	12.5	15	16	Volts	
V_{RD}	Reset Drain Voltage	13	13.5	14	Volts	
V_{LOAD}	Output Load Gate Voltage	0	1.6	3.0	Volts	
V_{PW}	P-Well Ground	0	0	0	Volts	
V_{SRC}	Output Amplifier Return	0	1.4	2.0	Volts	

CLOCK CHARACTERISTICS: $T_p = 20^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
$V_{\phi H(1,2)}$ HIGH	Horizontal Transport Clock HIGH	+ 4.5	+ 5.5	+ 6.5	Volts	
$V_{\phi H(1,2)}$ LOW	Horizontal Transport Clock LOW	- 0.2	0.0	+ 0.5	Volts	
$V_{\phi SW}$ HIGH	Summing Gate Clock HIGH	+ 4.5	+ 5.5	+ 6.5	Volts	
$V_{\phi SW}$ LOW	Summing Gate Clock LOW	- 0.2	0.0	+ 0.5	Volts	
$V_{\phi V(1,2)}$ HIGH	Vertical Transport Clocks HIGH	- 1.0	+ 0.0	+ 1.0	Volts	
$V_{\phi V(1,2)}$ LOW	Vertical Transport Clocks LOW	- 10	- 9	- 8	Volts	
$V_{\phi RG}$ HIGH	Reset Gate Clock HIGH	+ 6	+ 7	+ 8	Volts	
$V_{\phi RG}$ LOW	Reset Gate Clock LOW	+ 0.5	+ 2	+ 2.5	Volts	
$V_{\phi V1-TRI}$ HIGH	Vertical Tri-Level Clock HIGH	+ 9.0	+ 11.0	+ 17.0	Volts	

AC CHARACTERISTICS: $T_p = 20\text{ }^\circ\text{C}$ (Note 1)						
SYMBOL	PARAMETER	RANGE			UNIT	CONDITION
		MIN	TYPICAL	MAX		
V_{ODC}	Output DC Level	7.5	9.0	10	Volts	Note 6
R_o	Output load Resistor	0.7	1.0	1.5	$K\Omega$	
$f_{MAX\text{ HORIZ.}}$	Horizontal Clock Frequency		20	50	MHz	
P_D	On-Chip Power Dissipation		2.50		W	Note 7

NOTES

- 1.- T_p is defined as the package temperature.
- 2.- Standard test conditions are nominal clocks and DC operation voltages. 5.0 MHz horizontal data rate, integration time = 20.0 msec. Values shown are for 20 °C, unless otherwise indicated.
- 3.- Dark Current doubles every 5-7 °C.
- 4.- Excluding spikes.
- 5.- Excluding spikes, and measured @ $\frac{1}{2}V_{sat}$
- 6.- For the cases of $V_{RD} = \text{MIN, TYPICAL, MAX}$ and $R_o = 1\text{ k}\Omega$
- 7.- At $f_{MAX\text{ HORIZ.}} = 40\text{ MHz}$, 32 On-Chip amplifier outputs, vertical & horizontal registers.
- 8.- Device has 32 On-Chip amplifiers.

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

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