



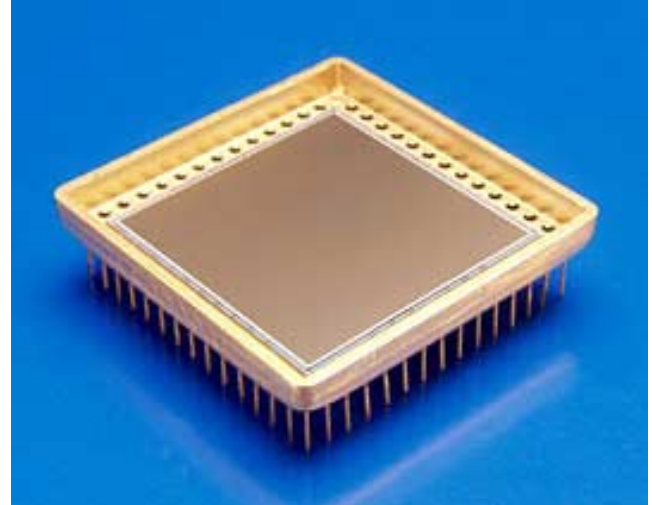
# CCD 442A

## 2048 x 2048 Element

### Full Frame Image Sensor

#### FEATURES

- 2048 x 2048 photosite array
- 15  $\mu\text{m}$  x 15 $\mu\text{m}$  pixel
- 30.72 mm x 30.72 mm image area
- Near 100% fill factor
- Multi-pinned phase (MPP) option
- Readout Noise less than 7 electrons at 250k pixels / sec
- Dynamic range: 10000:1
- Three phase buried channel NMOS



#### GENERAL DESCRIPTION

The CCD442A is a 2048 x 2048 element solid state Charge Coupled Device (CCD) Full Frame area image sensor which is intended for use in high-resolution scientific, industrial, and commercial electro-optical systems. The CCD442A is organized as a matrix array of 2048 horizontal by 2048 vertical CCD photosites. The pixel pitch and spacing is 15 $\mu\text{m}$ . For dark reference, the top and bottom eight rows and the left and right eight columns are covered by a light shield. The available imaging area is thus 2032 rows by 2032 columns.

The imaging array may be operated in one of two modes, Buried Channel or Multi-Pinned Phase (MPP). The Buried Channel operation offers low-noise performance and excellent charge transfer efficiencies. An additional implant under one vertical phase creates a virtual well which collects the photo-electrons with all Vertical clocks low during integration. This MPP mode decreases dark current down to 25 pA/cm<sup>2</sup> @ 25° C. Excellent low noise performance is achieved by use of the buried channel CCD structure and a dual stage low noise output amplifier with an output conversion of 3 $\mu\text{V}/\text{e}$ .

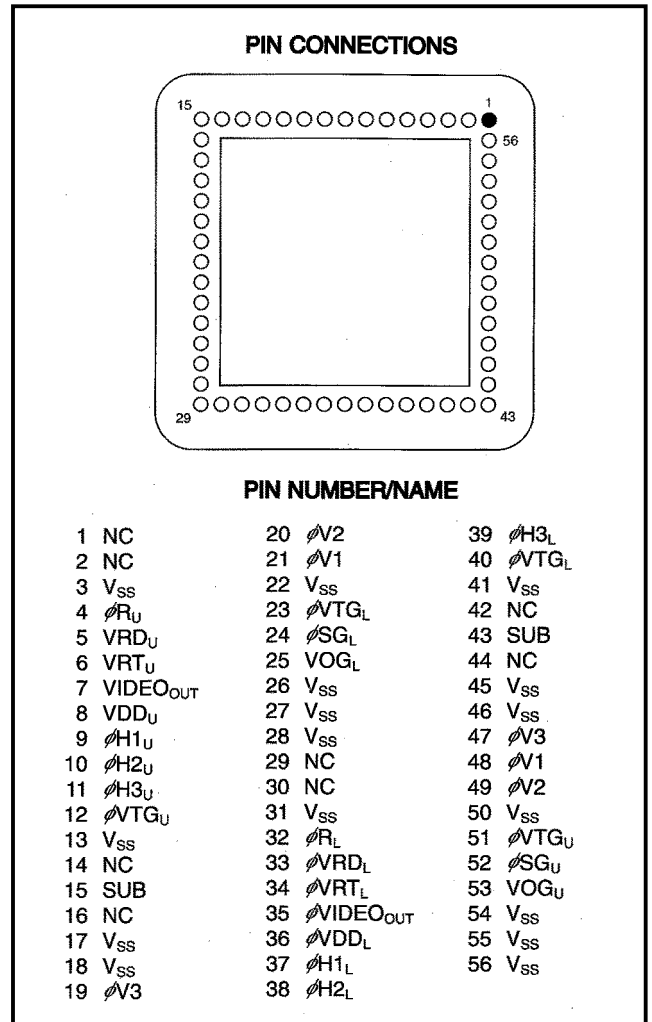
Device processing uses 2.5 micron design rules. The single metal, triple-poly process allows a photosite layout with smaller pixel geometries and fewer array blemishes.

#### FUNCTIONAL DESCRIPTION

The CCD442A consists of the following functional elements illustrated in the Block Diagram.

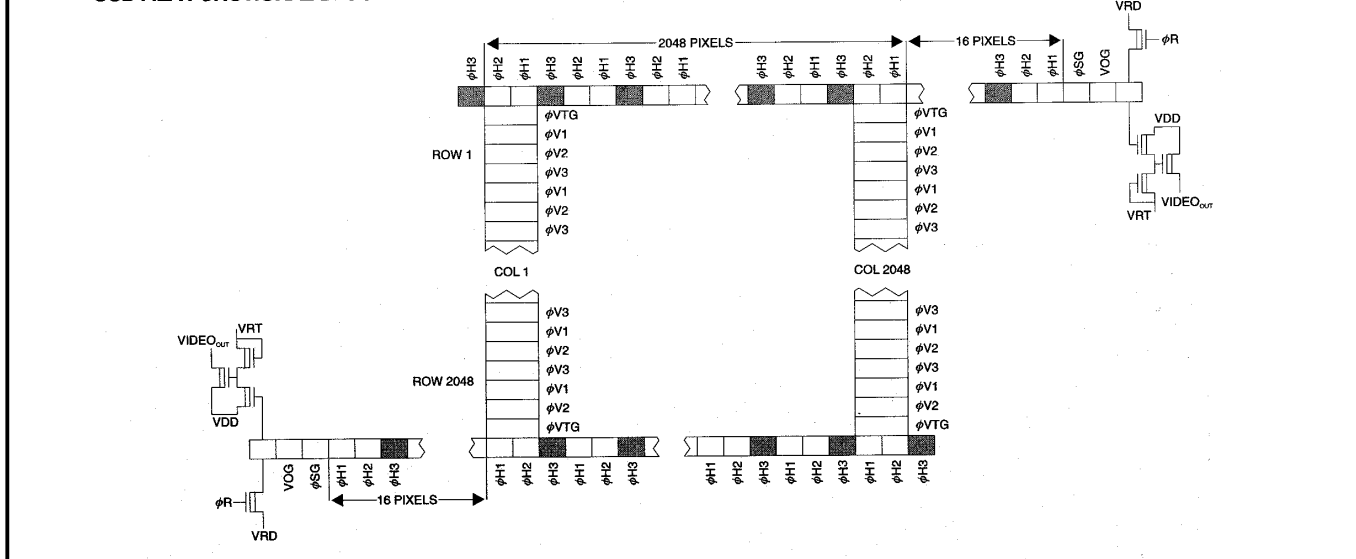
**Imaging Sensing Elements:** Incident photons pass through a transparent polycrystalline silicon gate structure creating electron hole pairs. The resulting photo-electrons are collected in the photosites during the integration period. The amount of charge accumulated in each photosite is a linear function of the localized incident illumination intensity and integration period.

The photosite structure is made up of contiguous CCD elements with no voids or inactive areas. In addition to sensing light, these elements are used to shift image data vertically. Consequently, the device needs to be shuttered during readout.



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## CCD442A FUNCTIONAL BLOCK DIAGRAM



**Vertical Charge Shifting:** The Full Frame architecture of the CCD 442A provides video information as a single sequential readout of 2048 lines containing 2048 photosite elements. At the end of an integration period the  $\phi V1$ ,  $\phi V2$ , and  $\phi V3$  clocks are used to transfer charge vertically through the CCD array to the horizontal readout register. Vertical columns are separated by a channel stop region to prevent charge migration. The CCD442A may be clocked such that the full array is readout the Upper or Lower Transport registers. The package pinouts are arranged so that the device may be rotated 180° without timing changes.

**The vertical transfer gate ( $\phi VTG$ )** is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation  $\phi VTG$  may be tied to  $\phi V3$ .

**Horizontal Charge shifting:**  $\phi H1$ ,  $\phi H2$ , and  $\phi H3$  are polysilicon gates used to transfer charge horizontally to the output amplifier. The horizontal transport register is twice the size of the photosite to allow for vertical binning. The array can be operated normally at full resolution or some lower resolution with binning.

The transfer of charge into the horizontal register is the result of a vertical shift sequence. This register has 16 additional register cells between the first pixel of each line and the output amplifier. The output from these locations contain no signal and may be used as a dark level reference.

The last clocked gate in the Horizontal registers is twice as large as the others and can be used to horizontally bin charge. This gate requires its own clock which may be tied to  $\phi H3$  for normal full resolution readout. The output video is available following the high to low transition of  $\phi SG$ .

**Output Amplifier:** The CCD442A has one output amplifier at the end of each horizontal register. They are dual FET floating diffusion amplifiers with a reset MOSFET tied to the input gate.

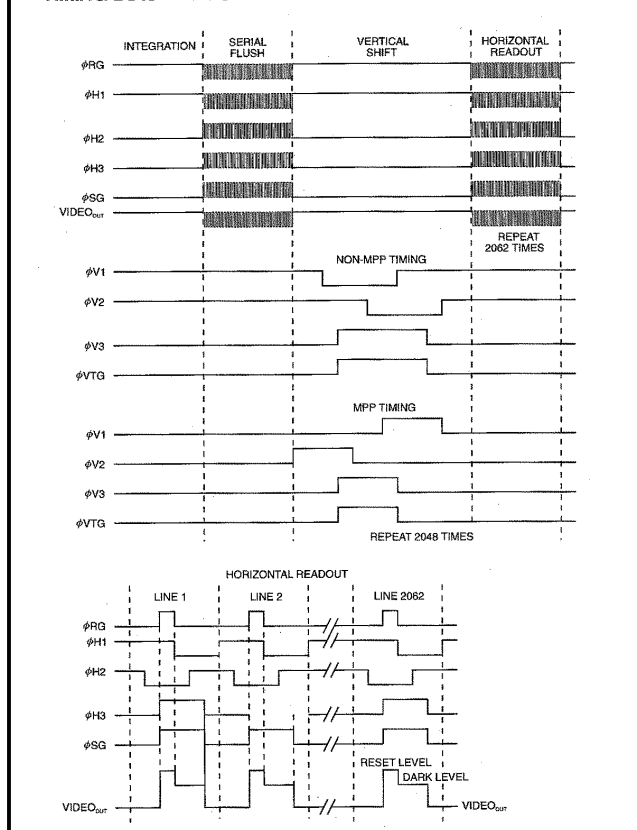
Charge packets are clocked to a precharge capacitor whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output  $V_{out}$  pin. The capacitor is reset with  $\phi R$  to a precharge level prior to the arrival of the next charge packet except when horizontally binning. It is reset by use of the reset MOSFET.

The output amplifier drain is tied to  $VDD$ . The source (Video Out) is

connected to an external load resistor to ground. The source constitutes the video output from the device.

**Multi-Pinned Phase:** MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an implant during the semiconductor manufacturing process. This implant creates a virtual well in the array which allows charge integration while maintaining pixel integrity with the Vertical clocks in the low state. Leaving the Vertical clocks in the low state during the integration cycle is the method used to implement MPP mode.

## TIMING DIAGRAM FOR LOWER OUTPUT OPERATION



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A drawback to utilizing the MPP mode is reduced full well capacity. The virtual well created by the MPP implant does not hold as much charge as the normal buried channel operating mode which leaves one Vertical clock in the high state during integration. The CCD442A may be operated in the conventional buried channel mode with increase in charge capacity over the MPP mode.

## DEFINITION OF TERMS

**Charge-Coupled Device** — A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

**Vertical Transport Clocks**  $\phi V_1, \phi V_2, \phi V_3$  — The clock signals applied to the vertical transport register.

**Horizontal Transport Clocks**  $\phi H_1, \phi H_2, \phi H_3$  — The clock signals applied to the horizontal transport register.

**Reset Clock**  $\phi R$  — The clock applied to the reset switch of the output amplifier.

**Dynamic Range** — The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

**Saturation Exposure** — The minimum exposure level that pro-

duces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the light intensity times the photosites integration time.

**Responsivity** — The output signal voltage per unit of exposure.

**Spectral Response Range** — The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

**Photo-Response Non-uniformity** — The difference of the response levels of the most and the least sensitive element under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

**Dark Signal** — The output signal in the dark caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

**Vertical Transfer Gate**  $\phi TG$  — Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

**Pixel** - A picture element or sensor element, also called photoelement or photosite.

### TYPICAL DC VOLTAGES

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
$V_{DD}$	DC Supply Voltage		22	25	V	
$V_{RD}$	Reset Drain Voltage	12	14	16		V
$V_{OG}$	Output Gate Voltage		0		V	
$V_{SS}$	Substrate Ground		0		V	
$V_{RT}$	Output Amplifier Load		3.0		V	

### TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V_{\phi H(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	
$V_{\phi V(1,2,3)}$	Vertical Array Clocks	+6.0	-8.0	V	
$V_{\phi R}$	Reset Array Clock	+10.0	0.0	V	
$V_{\phi VTG}$	Array Transfer Gate Clock	+6.0	-8.0	V	

Note:  $\phi H = 400\text{pF}$ ,  $\phi V = 60,000\text{pF}$

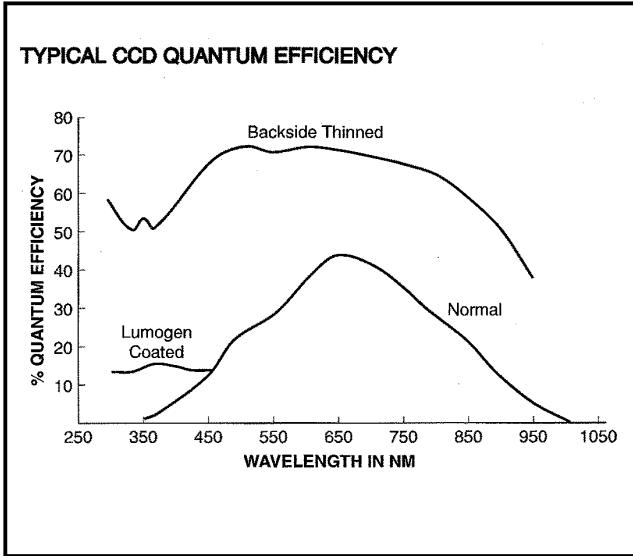
### TYPICAL DC VOLTAGES

SYMBOL	PARAMETER	RANGE			UNIT	REMARKS
		MIN	NOM	MAX		
$V_{SAT}$	Saturation Output Voltage Full Well Capacity Output Amp Sensitivity	300 100,000		600 200,000	mV e- $\mu V/e-$	Note 1
PRNU	Photo Response Non-Uniformity Peak-to-Peak		3.0	10	$\%V_{SAT}$	
DSNU	Dark Signal Non-Uniformity Peak-to-Peak			1.0	mV	
DC	Dark Current	0.025		2.0	nA/cm <sup>2</sup>	Note 2
R	Responsivity		1.0		$V\mu J/cm^2$	
$V_{ODC}$	Output DC Level		14.0		V	Note 3
Z	Suggested Load Register	1.0	5.0	20	k $\Omega$	Note 3

Note 1: Maximum well capacity is achieved operating in Buried Channel Mode, minimum capacity is in MPP mode.

Note 2: Values shown are for 25°C. Dark current doubles for every 5°-7°C.

Note 3: Standard test conditions are nominal MPP clocks and DC operating voltages. 1MHz Horizontal Data Rate.



**QUANTUM EFFICIENCY ENHANCEMENTS**

On a custom basis, our large area CCDs can be backside thinned for increased QE. The CCD is bump mated to a fanout and thinned to approximately 15 microns. The incident illumination enters through the backside of the array. Since no photons are absorbed in the polysilicon gate structures, the QE increases. WE can also coat frontside illuminated devices with a fluorescent dye that absorbs UV light and fluoresces in the visible range. This provides CCD response at wavelengths less than 400nm.

**COSMETIC GRADING**

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of  $V_{SAT}$  with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and for different device temperatures.

The CCD442A is available in various standard grades, as well as custom selected grades. Consult the factory for available grading information and custom selections.

**WARRANTY**

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

**CERTIFICATION**

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

