CCD424
1024 x 1024 Pixel Image Area
Split Frame Transfer CCD Sensor

FEATURES

- **1024 x 1024 Pixels Split Frame Transfer CCD**
- **21 µm x 21 µm Pixel**
- **21.50 mm x 21.50 mm Image Area**
- **11.13 mm x 21.50 mm (x2) Storage Areas**
- **100% Fill Factor**
- **Back Illuminated**
- **Bi-directional Serial Registers**
- **Gated Fast Dump Drains in Serial Registers**
- **Four Low Noise Output Amplifiers**
- **Three Phase Buried Channel CCD**

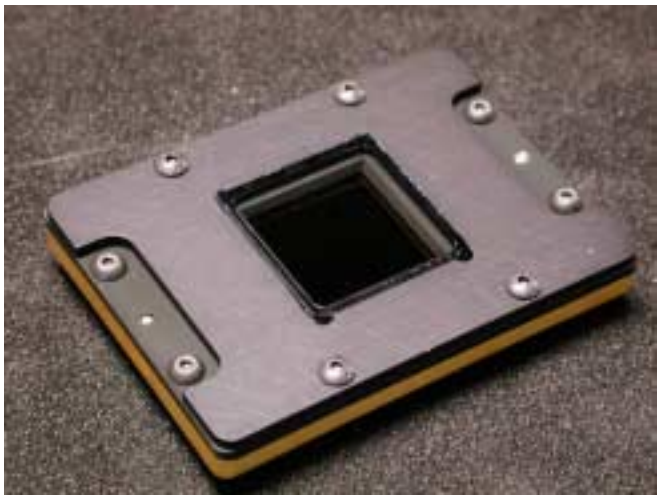
GENERAL DESCRIPTION

The CCD424 is a 1024 x 1024 split frame transfer CCD with 21µm pixels. The backside illuminated CCD is intended for advanced scientific, space, industrial, and commercial digital imaging applications. The split frame transfer architecture provides rapid image capture capability and the ability to read out from four output ports simultaneously further improves the imaging speed. The imaging array of the CCD424 consists of 1024 (H) by 1024 (V) pixels and the optically shielded frame storage regions, on the sides of the imaging array, are 530 (H) by 1024 (V) in dimensions. The vertical and horizontal CCD registers feature buried notch channels for improved CTE and radiation tolerance at low signal levels. There are 18 extra (overclocked) lines in each of the storage sections. The storage sections are connected to serial readout structures which are terminated with two single stage output amplifiers, one output at each end. Charge transfer is accomplished in the parallel and serial registers using three-phase clocks. The pixel pitch is 21 µm with a 100% fill factor. The imager operates in a back-illuminated mode for optimal sensitivity.

A single stage source follower output amplifier design was chosen for low noise performance. The read noise floor is less than 4 e^- at a pixel rate of 50 kHz.

The CCD424 is designed to operate between –30 °C and –100 °C.

The CCD424 is mounted in a 72-pin PGA package. The overall dimensions of the package are 2.88” (W) x 2.08” (L) x 0.24” (H).



Shown above is the back-illuminated CCD424 in its kovar package with a temporary protective window cover.

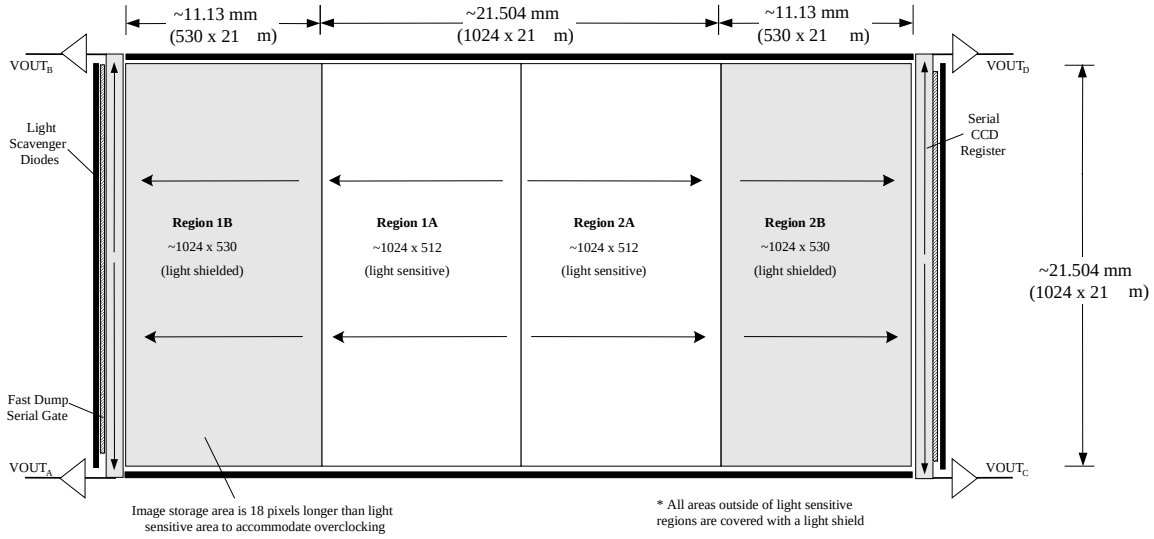
FUNCTIONAL DESCRIPTION

The following functional elements are illustrated in the block diagram shown below.

Image Sensing Elements:

The CCD424 operates in backside illuminated mode for optimal performance, thus, incident photons are collected on the backside of the CCD which has been thinned to about 20 microns. An accumulated back surface potential, accomplished by a special treatment of the backside surface helps directs the signal charge to the CCD depletion wells. A final antireflection coating is deposited to optimize the device sensitivity over specific spectral regions.

The imaging area is composed of contiguous CCD elements with no gaps or inactive areas. In addition to capturing and converting incident light into electrical charge, these elements are also used to shift the image charge from the imaging section to the storage areas.



CCD424 Block Diagram

Preliminary Preproduction Device Specifications

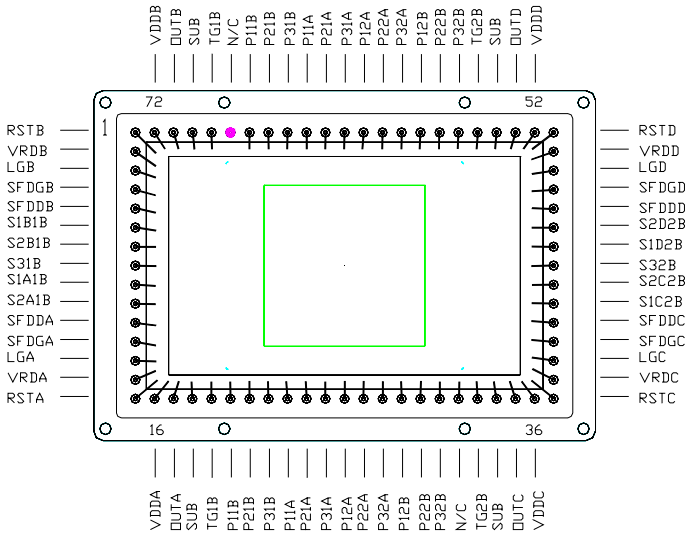
Vertical CCD Registers: The architecture of the CCD424 consists of a central photosensitive area of 1024 (H) x 1024 (V) pixels, which is electrically subdivided into two sections, each holding 512 (H) x 1024 (V) pixels. The imaging areas are connected to adjacent storage regions on each side. The storage areas are 530 (H) x 1024 (V) in dimensions. Charge transfer of 512 lines of 1024 photosensitive elements to the corresponding storage section is performed to store an image frame while the next frame is being integrated. Vertical columns are separated by channel stop regions to confine signal charge.

As described earlier, the imaging area is divided into two separate but identical segments, and each of the 512 (H) x 1024 (V) image section may be clocked in either direction.

The Vertical Transfer Gate (ΦVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ΦVTG may be tied to ΦV_3.

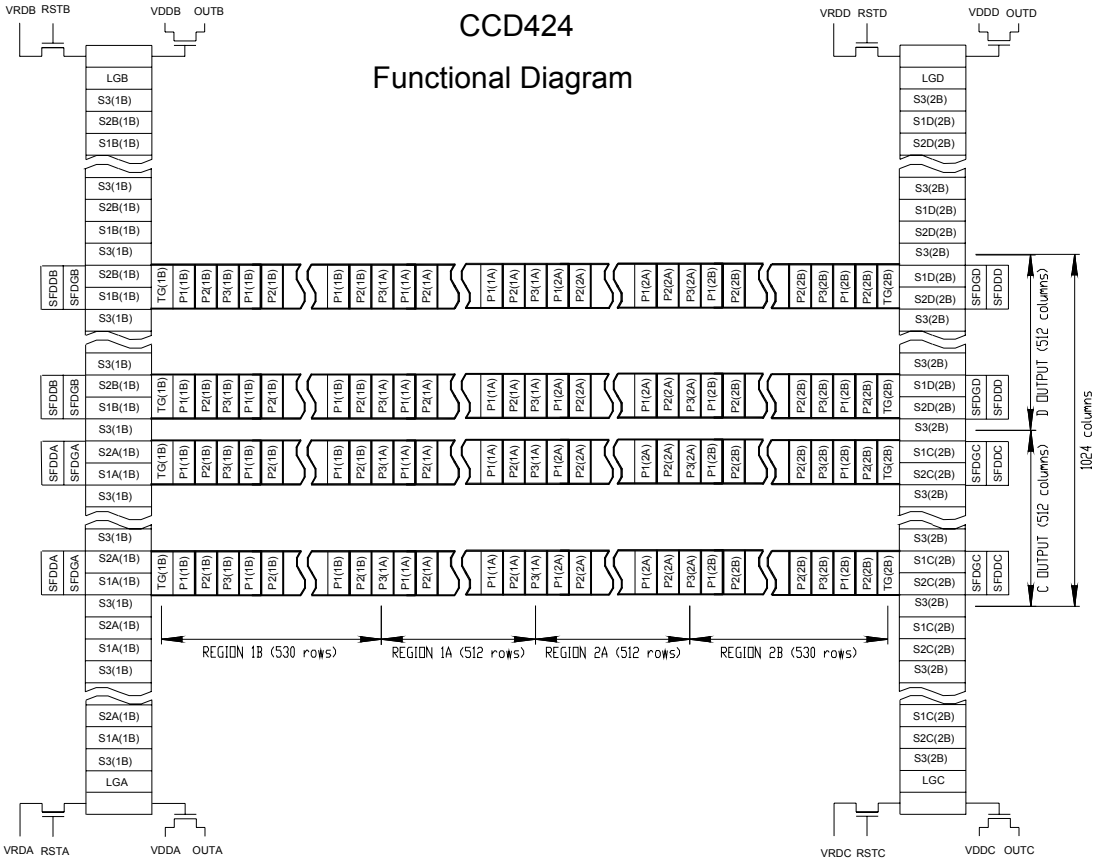
Horizontal CCD Registers: There are two horizontal registers, each with dedicated and electrically isolated input pins.Three-phase clocking is employed in the horizontal shift registers and bi-directional charge transport is possible. ΦH_1, ΦH_2, and ΦH_3 are polysilicon gate structures used to transfer the signal charge to the output amplifiers. In the normal mode of operation, at the end of the integration period, the signal in the imaging sections is transferred into the storage sections then the information in the storage sections is transferred to the horizontal registers sequentially, one line at a time. There are four additional prescan elements at each output.

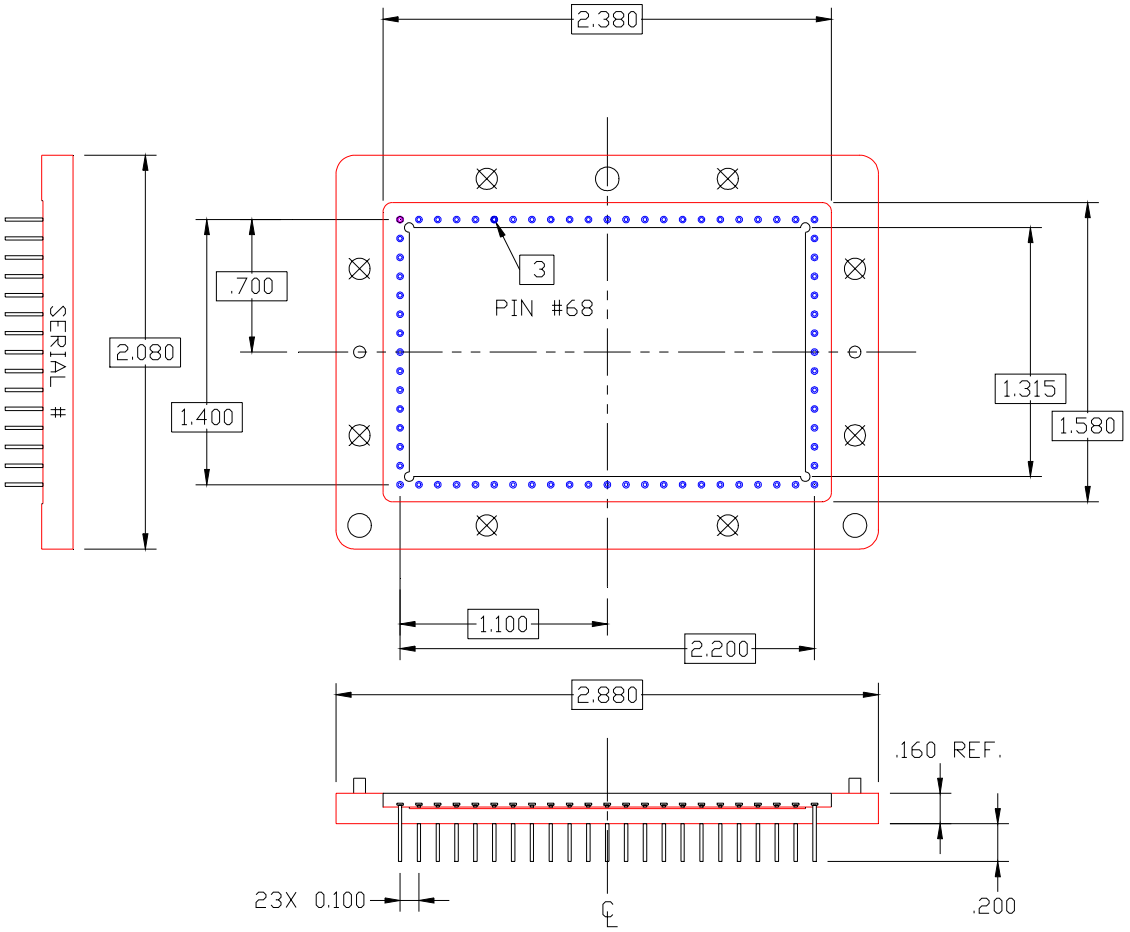
Fast Dump Drain: Fast dump gates and drains connected to the horizontal registers are provided to allow the signal charge in the horizontal registers to be completely discarded in a much faster manner compared to the normal read out rate.



CCD424 Pinout Diagram

Output Amplifiers: The CCD424 has a output amplifier at each end of the horizontal registers for a total of four output ports. They are single-stage floating diffusion amplifiers with a reset MOSFET tied to the input gate. Each output amplifier is equipped with a dedicated set of input and output signals. The image may be read out through one or two amplifiers per serial register, but in normal operation, both outputs of each horizontal register are used simultaneously.





CCD 424 Package Configuration

Charge packets are clocked to the output node, a pre-charged floating diffusion which potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The output node capacitor is reset with ΦR to a pre-charge level prior to the arrival of the next charge packet and it is reset by use of the reset MOSFET.

The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The source constitutes the video output from the device.

DEFINITION OF TERMS

Charge-Coupled Device A charge-coupled device is a monolithic silicon structure in which discrete packets of electron charge are transported from position to position by sequential clocking of an array of gates.

Vertical Transport Clocks ΦV_1, ΦV_2, ΦV_3 the clock signals applied to the vertical transport register.

Horizontal Transport Clocks ΦH_1, ΦH_2, ΦH_3 the clock signals applied to the horizontal transport registers.
Reset Clock ΦR the clock applied to the reset switch of the output amplifier.

Dynamic Range The ratio of saturation output voltage to RMS noise in the dark. The peak-to-peak random noise is 4-6 times the RMS noise output.

Saturation Exposure The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity The output signal voltage per unit of exposure.

Photo-Response Non-Uniformity The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal The output signal in the caused by thermally generated electrons. Dark signal is a linear function of integration time and an exponential function of chip temperature.

Vertical Transfer Gate ΦVTG Gate structures adjacent to the end row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically through the array. Upon reaching the end row of photosites, the charge is transferred in parallel via the transfer gates to the horizontal transport shift registers whenever the transfer gate voltage goes low.

Pixel Picture element or sensor element, also called photoelement or photosite.

CCD424 IMAGE SENSOR CHARACTERISTICS AND PERFORMANCE SPECIFICATIONS

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{DD}	DC Supply Voltage	23	24	25	V	
V_{RD}	Reset Drain Voltage	12	13	15	V	
V_{LG}	Last Gate	-4	-3	-2	V	
V_{SS}	Substrate Ground		0		V	
SFDD	Serial Fast Dump Drain	23	24	25	V	
SFDG ON	Serial Fast Dump Gate	8	9	10	V	
SFDG OFF	Serial Fast Dump Gate	-9	-8	-7	V	

TYPICAL CLOCK VOLTAGES AND CHARACTERISTICS

SYMBOL	PARAMETER	HIGH	LOW	UNIT	REMARKS
$V\Phi_{V(1,2,3)}$	Vertical Array Clocks	+5.0	-8.0	V	
C_{P1-3}	Region 1A/2A, 1B/2B Capacitance	18500		pF/phase	
TG	Transfer Gate	+5.0	-8.0	V	
C_{TG}	Transfer Gate Capacitance	200		pF/phase	
$V\Phi_{H(1,2,3)}$	Horizontal Multiplexer Clock	+5.0	-5.0	V	Typical horizontal clock frequency range is 200 – 400 kHz
C_{H1-3}	Horizontal Clock Capacitance	220		pF/phase	
$V\Phi_{R}$	Reset Array Clock	+9.0	0.0	V	
C_{RST}	Reset clock capacitance	120		pF/phase	

Note: All clock rise and fall times should be 10 ns.

AC CHARACTERISTICS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{ODC}	Output DC Level		14.0		V	
Z	Suggested Load Resistor	5	10	20	K	

PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{SAT}	Saturation Output Voltage		1500		mV	
FW_{PAR}	Full Well Capacity Parallel Registers		450		ke-	
FW_{HOR}	Full Well Capacity Horizontal Registers		500		ke-	
CTE_{PAR}	Charge Transfer Efficiency Parallel Registers		0.99999		#	
CTE_{HOR}	Charge Transfer Efficiency Horizontal Registers		0.99999		#	
QE	Quantum Efficiency 300 nm 400 nm 500 nm 600 nm 700 nm 800 nm 900 nm		 50 70 85 90 85 60 40		%	
OCG	Output Amplifier Conversion Gain		3.5		V/e-	
PRNU	Photo Response Non-Uniformity, Peak-to-Peak		10.0		$\%V_{SAT}$	
DC	Dark Current	2		500	e-/pix/sec	Note 1

Note 1: Values shown are at –100 °C and –30 °C. Dark current doubles about every 8 °C.

COSMETIC GRADING

Device grading helps to establish a ranking for the image quality that a CCD will provide. Blemishes are characterized as spurious pixels exceeding 10% of V_{SAT} with respect to neighboring elements. Blemish content is determined in the dark, at various illumination levels and at different operating temperatures.

The CCD424 is available in several different grades, as well as custom selected grades. Consult Sales representative for available grading information and custom selections.

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

Fairchild Imaging, Inc. 1801 McCarthy Blvd., Milpitas, CA 95035
(800) 325-6975, (408) 433-2500